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SM 1 SM 1 EECE 488 Set 1: Introduction and Background. EECE488: Analog CMOS Integrated Circuit Design Introduction and Background. Shahriar Mirabbasi Department of Electrical and Computer Engineering University of British Columbia shahriar@ece.ubc.ca. Technical contributions of Pedram Lajevardi in revising the slides is greatly acknowledged.

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Design of Analog CMOS Integrated Circuits by B. Razavi, McGraw Hill. 2. CMOS Circuit design, Layout & Simulation by Baker, Li & Boyce, IEEE Press, 1998. 3. Analysis and Design of Analog Integrated Circuits, Gray, Hurst, Lewis and Meyer, John Wiley & Sons, 2003. 4. Analog VLSI Signal and Information Processing, Ismail and Faiz, McGraw-Hill. 5.

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Design of Analog CMOS Integrated Circuits Behzad Razavi Errata p. 6, Section 1.3, first sentence should read: The idea of metal-oxide-semiconductor ...

Design of Analog CMOS Integrated Circuits - Engineering

to the design of a comparator. Random circuit noise can cause the output to change from one logic level to the other, even when the comparator input is held constant. Hence, in order to measure the input offset voltage in the presence of circuit noise, one would look for the input voltage that results in

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Analog Integrated Circuit Design - Engineering

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In Chapter 4, the important topics of current mirrors and active loads are considered. These configurations are basic building blocks in modern analog IC design, and this material should be covered in full, with the exception of the material on band-gap references and the material in the appendices.

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Systematic Design of Analog CMOS Circuits : Paul G. A

EECE488: Analog CMOS Integrated Circuit Design 3. Single-Stage Amplifiers Shahriar Mirabbasi Department of Electrical and Computer Engineering University of British Columbia shahriar@ece.ubc.ca Technical contributions of Pedram Lajevardi in revising the course notes are greatly acknowledged.

EECE488: Analog CMOS Integrated Circuit Design 3. Single

Title: Systematic Design of Analog Circuits Using Pre-Computed Lookup Tables Speakers: Paul Jespers and Boris Murmann Abstract The majority of textbook material on analog circuit design is based on the square-law model for MOS transistors. While this model remains useful for teaching, it has become too inaccurate for design in nano-scale CMOS.

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Electronic noise estimates and countermeasures Design of Analog CMOS integrated circuits, Bahzad Razavi, Chapter 7 - Noise Thermic noise: Represented as parallel current at the output. Using $\hat{I}^3=2/3$. (For small linewidths, 250nm and below, \hat{I}^3 may be 2-3.)

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